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CHENG, PETER L	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

mailroom@bskb.com

Office Action Summary	Application No.	Applicant(s)	
	10/623,645	WANG ET AL.	
	Examiner	Art Unit	
	Peter L. Cheng	2625	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 July 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description:

- **Fig. 3** references **2a, 2b, 2c**;

Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

2. The disclosure is objected to because of the following informalities:

- **Page 7, line 1:** since **pixel array** is not previously mentioned in the specification, suggest changing **the pixel array** to **a pixel array**;

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claim 3 is rejected under 35 U.S.C. 102(e) as being anticipated by **NOSE [US Patent Application 2002/0163490 A1]**.

As for claim 3, NOSE teaches a data driver of a display **[Fig. 1** illustrates an LCD display driver**]** forming an image frame by sequentially scanning horizontal lines **[Fig. 2**

illustrates the horizontal scanning of image data corresponding to the primary colors, red, green and blue**]**, the data driver comprising:

> **a shift register receiving and outputting image data of the three primary colors *in a sequence* of the primary colors within a scan duration of one of the horizontal lines**
>
> **[Fig. 3** "shift register section" **63** and "data register section" **64** correspond to a "*shift register receiving and outputting image data*"; the "shift register section" aligns the incoming gray-scale data (D1, D2, or D3) into the "data register section";
>
> NOSE explains, "the gray-scale data being fed from the display control circuit 3, for example, 6 bits of gray-scale data D1, D2, and D3 are held in parallel by the data register section 64 which is controlled by an output at each stage in a shift register section 63 that is controlled by a horizontal start pulse HSP and a clock signal HCK"; **page 6, paragraph 83, lines 4 – 9.**
>
> NOSE further teaches, "The gray-scale data for the R color, gray-scale data for the G color, and gray-scale data for the B color, all being fed from the display control circuit 3, are sequentially switched in a repeated manner in every scanning position, as shown in Fig. 2. Moreover, in this example, gray-scale data D1, D2, and D3 are transferred to the data register section 64 of the signal

line driving circuit 6 through three ports, as shown in Fig. 3"; **page 7, paragraph 83, lines (starting on page 7) 6 – 8.**

Fig. 2 illustrates a "scan duration of one horizontal line" consisting of red image "signal line" data which is then followed, in sequence, by green "signal line" image data, and then blue "signal line" image data**];**

a sample and hold register acquiring the image data from the shift register [Fig. 3 "data register section" **64** and "latch section" **65** correspond to the "sample and hold register";

As noted above, NOSE teaches, "the gray-scale data being fed from the display control circuit 3, for example, 6 bits of gray-scale data D1, D2, and D3 are held in parallel by the data register section 64 which is controlled by an output at each stage in a shift register section 63 that is controlled by a horizontal start pulse HSP and a clock signal HCK"; **page 6, paragraph 83, lines 4 – 9.**

Nose further teaches, "The signals making up gray-scale data D1, D2, and D3 being held in parallel in the data register section 64 are collectively transferred by a latch signal STB to a latch section 65 and latched therein"; **page 6, paragraph 83, lines 9 - 12];**

a gamma multiplexer outputting gamma reference voltages for the primary color in the sequence of the primary colors

[Fig. 3 "RGB switching reference gray-scale voltage producing circuit" **4** contains a multiplexer consisting of multiplexers **M1, M2, ..., M10** which is controlled by a common signal **SL**;

NOSE cites," voltages obtained by selecting from voltages V0R, V0G, V0B, ..., V9R, V9G, and V9B which are obtained by dividing a reference voltage V_{REF} using a voltage dividing circuit for a R color (DR), a voltage dividing circuit for a G color (DG), and a voltage dividing circuit for a B color (DB), respectively, for every color of the R, G, and B colors in accordance with a selection control signal SL using MPXs (multiplexers) M1, M2, ..., M9, and M10, are output, through voltage followers B1, B2, ..., B9, and B10, as reference gray-scale voltages V0, V1, V1, ..., V8, and V9"; **page 6, paragraph 82, lines 2 – 12.** "Each of the MPXs M1, M2, ..., M9, and M10 selects a corresponding voltage in response to the selection control signal SL being output in synchronization with the selection of the scanning line 21 for each of the R, G, and B colors and outputs it as the reference gray-scale voltage to the signal line driving circuit 6"; **page 6, paragraph 82, lines 15 – 20];**

a digital-to-analog converter for gamma calibration, receiving the image data from the sample and hold register and the gamma reference voltages

from the gamma multiplexer, and outputting calibrated image signals of the three primary colors

[Fig. 3 "DAC" **62** is a digital-to-analog converter which receives the image data from the sample-and-hold register ("data register section" **64** and "latch section" **65**) after the data is passed through a "level shift section 66" **[page 6, paragraph 83, lines 14 – 15]**. The DAC reference voltage, for each of the three primary colors - red, green, and blue, is provided through multiplexer **61.** "Gray-scale data D1, D2, and D3 having been transferred to the DAC 62 undergo the gamma correction based on the set of the reference gray-scale voltages V0 to V4 and the set of the reference gray-scale voltages V5 to V9 fed from the MPX 61, and at the same time, causes a D/A converted signal voltage to be generated which is output through the voltage followers F1, F2, ..., F639, and F640 to each of the corresponding signal lines 22"; **page 6, paragraph 83, line 15 – page 7, paragraph 83, line (starting on page 7) 6];**

and a buffer receiving the calibrated image signals from the digital-to-analog converter and outputting the calibrated image signals in the sequence of the primary colors

[Fig. 3 "voltage followers" **F1, F2, ..., F640** correspond to the "buffer receiving the calibrated image signals from the digital-to-analog converter"**].**

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

7. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over **NOSE [US Patent Application 2002/0163490 A1]** in view of *prior art* taught by NOSE.

As for claim 1, NOSE teaches *prior art* in which a data driver of a display **[Fig. 10** illustrates an LCD display driver**]** forming an image frame by sequentially scanning horizontal lines **[Fig. 12** illustrates the horizontal scanning of image data corresponding to the primary colors, red, green and blue**]**, the data driver comprising:

a shift register receiving image data of three primary colors in serial and ***outputting the image data of the three primary colors in parallel*** **within each**

of scan durations of the horizontal lines

[Fig. 11 "shift register section" **163** and "data register section" **164** hold image data for red, green and blue channels *simultaneously*;

NOSE cites, "6 bits of R-color gray-scale data DR, 6 bits of G-color gray-scale data DG, and 6 bits of B-color gray-scale data DB all being fed from the display control circuit 13 are held, in parallel, in a data register section 164 being controlled by an output, which is controlled by a horizontal start pulse HSP and a clock signal HCK, fed at each stage in a shift register section 163" **page 2, paragraph 12, lines 1 - 7];**

a sample and hold register acquiring the image data from the shift register

[Fig. 11 "data register section" **164** and "latch section" **165** correspond to the "sample and hold register";

NOSE teaches, "The ... gray-scale data DR, DG, and DB" (which are not the same as DR, DG and DB shown in Fig. 3) "being held in parallel in the data register section 164 are transferred collectively to a latch section 165 by a latch signal STB and then are latched therein"; **page 2, paragraph 12, lines 7 – 11];**

three digital-to-analog converters for gamma calibration, receiving the image data of the three primary colors from the sample and hold register

[Fig. 11 "DAC" **162** is a digital-to-analog converter which receives the image data from the sample-and-hold register ("data register section" **164** and "latch section" **165**) after the data is passed through a "level shift section 166" **[page 2, paragraph 12, lines 12 – 13]**.

Although shown as one digital-to-analog converter (for all three primary colors – red, green and blue), configuring three separate analog-to-digital converters, one for each primary color, is equivalent**];**

and *three buffers respectively receiving the calibrated image signals of the three primary colors from the three digital-to-analog converters*, in the sequence of the primary colors

[Fig. 11 "voltage followers" **F1, F2, ..., F1920** are the separate buffers for each color (red, green, blue) pixel (in a horizontal scan). NOSE cites, "Fig. 11 shows an example in which voltages corresponding to the gray-scale data are output to 1920 pieces of the pixel electrodes 123 corresponding to 640 pieces of color pixels arranged in a horizontal direction in a liquid crystal panel 12"; **page 2, paragraph 11, lines 3 – 7.**

Although shown as 1920 separate buffers (one for each color pixel), partitioning these 1920 separate buffers as three groups of buffers, one for each primary color, is equivalent**].**

However, with respect to the embodiment of the invention for this immediate claim, NOSE does not specifically teach limitations

> ***a gamma multiplexer outputting gamma reference voltages for the three primary colors in a sequence of the primary colors within each of the scan durations of the horizontal lines***;
>
> *and*
>
> **three digital-to-analog converters for gamma calibration, receiving the image data of the three primary colors from the sample and hold register *with the gamma reference voltages for the three primary colors from the gamma multiplexer*, and outputting calibrated image signals of the three primary colors, respectively;**

However, as noted for the embodiment of the invention in claim 3, and as shown in **Fig. 3**, NOSE teaches a

> **a gamma multiplexer outputting gamma reference voltages for the three primary colors *in a sequence of the primary colors within each of the scan durations of the horizontal lines***;

Fig. 3 "RGB switching reference gray-scale voltage producing circuit" **4** contains a multiplexer consisting of multiplexers **M1, M2, ..., M10** which is controlled by a common signal **SL**;

NOSE cites," voltages obtained by selecting from voltages V0R, V0G, V0B, ..., V9R, V9G, and V9B which are obtained by dividing a reference voltage V_{REF} using a voltage dividing circuit for a R color (DR), a voltage dividing circuit for a G color (DG), and a voltage dividing circuit for a B color (DB), respectively, for every color of the R, G, and B colors in accordance with a selection control signal SL using MPXs (multiplexers) M1, M2, ..., M9, and M10, are output, through voltage followers B1, B2, ..., B9, and B10, as reference gray-scale voltages V0, V1, V1, ..., V8, and V9"; **page 6, paragraph 82, lines 2 – 12.** "Each of the MPXs M1, M2, ..., M9, and M10 selects a corresponding voltage in response to the selection control signal SL being output in synchronization with the selection of the scanning line 21 for each of the R, G, and B colors and outputs it as the reference gray-scale voltage to the signal line driving circuit 6"; **page 6, paragraph 82, lines 15 – 20.**

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine NOSE's teachings of the instant application's claim 3 (i.e., the "***gamma multiplexer***" or "RGB switching reference gray-scale voltage producing circuit") with the *prior art* taught by NOSE if the timing requirements necessitated simultaneous driving of the primary colors – red, green and blue.

With the *substitution* of the "RGB switching reference gray-scale voltage producing circuit" shown in **Fig. 3** (reference number **4**) in place of the "reference gray-scale voltage producing circuit" shown in **Fig. 11** (reference number **14**), it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide ***gamma reference voltages for the three primary colors from the gamma multiplexer***.

8. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over **NOSE [US Patent Application 2002/0163490 A1]** in view of **ZAVRACKY [US Patent Application 2001/0054989 A1]** and in view of *prior art* taught by NOSE.

As for claim 2, NOSE teaches *prior art* in which a data driver of a display **[Fig. 10** illustrates an LCD display driver**]** forming an image frame by sequentially scanning horizontal lines **[Fig. 12** illustrates the horizontal scanning of image data corresponding to the primary colors, red, green and blue**]**, the data driver comprising:

> **a shift register receiving image data of three primary colors in serial and *outputting the image data of the three primary colors in parallel* within each of scan durations of the horizontal lines**
>
> **[Fig. 11** "shift register section" **163** and "data register section" **164** hold image data for red, green and blue channels *simultaneously*;

NOSE cites, "6 bits of R-color gray-scale data DR, 6 bits of G-color gray-scale data DG, and 6 bits of B-color gray-scale data DB all being fed from the display control circuit 13 are held, in parallel, in a data register section 164 being controlled by an output, which is controlled by a horizontal start pulse HSP and a clock signal HCK, fed at each stage in a shift register section 163" **page 2, paragraph 12, lines 1 - 7];**

a sample and hold register acquiring the image data of the three primary colors from the shift register

[Fig. 11 "data register section" **164** and "latch section" **165** correspond to the "sample and hold register";

NOSE teaches, "The ... gray-scale data DR, DG, and DB" (which are not the same as DR, DG and DB shown in Fig. 3) "being held in parallel in the data register section 164 are transferred collectively to a latch section 165 by a latch signal STB and then are latched therein"; **page 2, paragraph 12, lines 7 – 11];**

However, with respect to the embodiment of the invention for this immediate claim, NOSE does not specifically teach limitations

[1] ***a first multiplexer receiving the image data of the three primary colors from the sample and hold register and outputting them in a sequence of the primary colors within each of the scan durations of the horizontal lines***;

[2] a second multiplexer outputting gamma reference voltages for the three primary colors *in the sequence of the primary colors within each of the scan durations of the horizontal lines*;

[3] a digital-to-analog converter for gamma calibration, receiving the image data *from the first multiplexer and the gamma reference voltages from the second multiplexer*, and outputting calibrated image signals of the three primary colors;

and [4] *a buffer receiving the calibrated image signals from the digital-to-analog converter and outputting the calibrated image signals in the sequence of the primary colors;*

Regarding limitation **[1]**, ZAVRACKY teaches a method of multiplexing the "image data of the three primary colors". From **Fig. 15A,** ZAVRACKY teaches, "The 8-bit output from the multiplexers 730R, 730G, 730B are received by a 3:1 RGB multiplexer 740. The three colors are time sequenced by the RGB multiplexer 740 to yield a 24-bit digital signal"; **page 9, paragraph 123, lines 3 – 6.**

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of ZAVRACKY with those of NOSE by adding a

"***first multiplexer receiving the image data of the three primary colors***" from the sample and hold register as this would reduce the number of "digital-to-analog" and "buffer" functional blocks resulting in lower hardware cost.

Regarding limitation **[2]**, as noted for the embodiment of the invention in claim 3, and as shown in **Fig. 3**, NOSE teaches

> **a second multiplexer outputting gamma reference voltages for the three primary colors *in the sequence of the primary colors within each of the scan durations of the horizontal lines*;**

Fig. 3 "RGB switching reference gray-scale voltage producing circuit" **4** contains a multiplexer consisting of multiplexers **M1, M2, ..., M10** which is controlled by a common signal **SL**;

NOSE cites," voltages obtained by selecting from voltages V0R, V0G, V0B, ..., V9R, V9G, and V9B which are obtained by dividing a reference voltage V_{REF} using a voltage dividing circuit for a R color (DR), a voltage dividing circuit for a G color (DG), and a voltage dividing circuit for a B color (DB), respectively, for every color of the R, G, and B colors in accordance with a selection control signal SL using MPXs (multiplexers) M1, M2, ..., M9, and M10, are output, through voltage followers B1, B2, ..., B9, and B10, as reference gray-scale voltages V0, V1, V1, ..., V8, and V9"; **page 6, paragraph 82, lines 2 – 12.** "Each of the MPXs M1, M2, ..., M9, and M10 selects a corresponding voltage in

response to the selection control signal SL being output in synchronization with the selection of the scanning line 21 for each of the R, G, and B colors and outputs it as the reference gray-scale voltage to the signal line driving circuit 6"; **page 6, paragraph 82, lines 15 – 20.**

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine NOSE's teachings of the instant application's claim 3 (i.e., the "***gamma multiplexer***" or "RGB switching reference gray-scale voltage producing circuit") with the teachings of ZAVRACKY (i.e., the addition of a multiplexer between the sample-and-hold register and digital-to-analog converter) and the *prior art* taught by NOSE so as to reduce the number of "digital-to-analog" and "buffer" functional blocks resulting in lower hardware cost.

Regarding limitation **[3]**, as noted for the embodiment of the invention in claim 3, and as shown in **Fig. 3**, NOSE teaches

> **a digital-to-analog converter for gamma calibration, receiving the image data *from the first multiplexer and the gamma reference voltages from the second multiplexer*, and outputting calibrated image signals of the three primary colors;**

Fig. 3 "DAC" **62** is a digital-to-analog converter which receives the image data from the sample-and-hold register ("data register section" **64** and "latch section" **65**) after the

data is passed through a "level shift section 66" **[page 6, paragraph 83, lines 14 – 15]**. The DAC reference voltage, for each of the three primary colors - red, green, and blue, is provided through multiplexer **61.** "Gray-scale data D1, D2, and D3 having been transferred to the DAC 62 undergo the gamma correction based on the set of the reference gray-scale voltages V0 to V4 and the set of the reference gray-scale voltages V5 to V9 fed from the MPX 61, and at the same time, causes a D/A converted signal voltage to be generated which is output through the voltage followers F1, F2, ..., F639, and F640 to each of the corresponding signal lines 22"; **page 6, paragraph 83, line 15 – page 7, paragraph 83, line (starting on page 7) 6.**

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine NOSE's teachings of the instant application's claim 3 (i.e., "***a digital-to-analog converter for gamma calibration***") with the teachings of ZAVRACKY (i.e., the addition of a multiplexer between the sample-and-hold register and digital-to-analog converter) and the *prior art* taught by NOSE so as to reduce the number of "digital-to-analog" and "buffer" functional blocks resulting in lower hardware cost.

Regarding limitation **[4]**, as noted for the embodiment of the invention in claim 3, and as shown in **Fig. 3**, NOSE teaches

a buffer receiving the calibrated image signals from the digital-to- analog converter and outputting the calibrated image signals in the sequence of the primary colors;

Fig. 3 "voltage followers" **F1, F2, ..., F640** correspond to the "buffer receiving the calibrated image signals from the digital-to-analog converter".

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine NOSE's teachings of the instant application's claim 3 (i.e., "***a buffer receiving the calibrated image signals from the digital-to-analog converter***") with the teachings of ZAVRACKY (i.e., the addition of a multiplexer between the sample-and-hold register and digital-to-analog converter) and the *prior art* taught by NOSE so as to reduce the number of "digital-to-analog" and "buffer" functional blocks resulting in lower hardware cost.

9. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over **NOSE [US Patent Application 2002/0163490 A1]** in view of **HERRMANN [US Patent Application 2003/0197674 A1]**.

As for claim 4, NOSE teaches a data driver of a display **[Fig. 1** illustrates an LCD display driver**]** forming an image frame ~~***composed of sub-frames of three primary colors***~~ by sequentially scanning horizontal lines ~~***for each sub-frame***~~ **[Fig. 2** illustrates

the horizontal scanning of image data corresponding to the primary colors, red, green and blue**]**, the data driver comprising:

> **a shift register receiving and outputting image data of one of the three primary colors within each of scan durations of the horizontal lines**
>
> **[Fig. 3** "shift register section" **63** and "data register section" **64** correspond to a "*shift register receiving and outputting image data*"; the "shift register section" aligns the incoming gray-scale data (D1, D2, or D3) into the "data register section";
>
> NOSE explains, "the gray-scale data being fed from the display control circuit 3, for example, 6 bits of gray-scale data D1, D2, and D3 are held in parallel by the data register section 64 which is controlled by an output at each stage in a shift register section 63 that is controlled by a horizontal start pulse HSP and a clock signal HCK"; **page 6, paragraph 83, lines 4 – 9.**
>
> NOSE further teaches, "The gray-scale data for the R color, gray-scale data for the G color, and gray-scale data for the B color, all being fed from the display control circuit 3, are sequentially switched in a repeated manner in every scanning position, as shown in Fig. 2. Moreover, in this example, gray-scale data D1, D2, and D3 are transferred to the data register section 64 of the signal line driving circuit 6 through three ports, as shown in Fig. 3"; **page 7, paragraph 83, lines (starting on page 7) 6 – 8.**

Fig. 2 illustrates a "scan duration of one horizontal line" consisting of red image "signal line" data which is then followed, in sequence, by green "signal line" image data, and then blue "signal line" image data**];**

a sample and hold register acquiring the image data from the shift register [Fig. 3 "data register section" **64** and "latch section" **65** correspond to the "sample and hold register";

As noted above, NOSE teaches, "the gray-scale data being fed from the display control circuit 3, for example, 6 bits of gray-scale data D1, D2, and D3 are held in parallel by the data register section 64 which is controlled by an output at each stage in a shift register section 63 that is controlled by a horizontal start pulse HSP and a clock signal HCK"; **page 6, paragraph 83, lines 4 – 9.**

Nose further teaches, "The signals making up gray-scale data D1, D2, and D3 being held in parallel in the data register section 64 are collectively transferred by a latch signal STB to a latch section 65 and latched therein"; **page 6, paragraph 83, lines 9 - 12];**

a gamma multiplexer outputting gamma reference voltages for the primary color to which the image data from the shift register belongs

[Fig. 3 "RGB switching reference gray-scale voltage producing circuit" **4** contains a multiplexer consisting of multiplexers **M1, M2, ..., M10** which is controlled by a common signal **SL**;

NOSE cites," voltages obtained by selecting from voltages V0R, V0G, V0B, ..., V9R, V9G, and V9B which are obtained by dividing a reference voltage V_{REF} using a voltage dividing circuit for a R color (DR), a voltage dividing circuit for a G color (DG), and a voltage dividing circuit for a B color (DB), respectively, for every color of the R, G, and B colors in accordance with a selection control signal SL using MPXs (multiplexers) M1, M2, ..., M9, and M10, are output, through voltage followers B1, B2, ..., B9, and B10, as reference gray-scale voltages V0, V1, V1, ..., V8, and V9"; **page 6, paragraph 82, lines 2 – 12.** "Each of the MPXs M1, M2, ..., M9, and M10 selects a corresponding voltage in response to the selection control signal SL being output in synchronization with the selection of the scanning line 21 for each of the R, G, and B colors and outputs it as the reference gray-scale voltage to the signal line driving circuit 6"; **page 6, paragraph 82, lines 15 – 20];**

a digital-to-analog converter for gamma calibration, receiving the image data from the sample and hold register and the gamma reference voltage from the gamma multiplexer, and outputting a calibrated image signal

[Fig. 3 "DAC" **62** is a digital-to-analog converter which receives the image data from the sample-and-hold register ("data register section" **64** and "latch section" **65**) after the data is passed through a "level shift section 66" **[page 6, paragraph 83, lines 14 – 15]**. The DAC reference voltage, for each of the three primary colors - red, green, and blue, is provided through multiplexer **61.** "Gray-scale data D1, D2, and D3 having been transferred to the DAC 62 undergo the gamma correction based on the set of the reference gray-scale voltages V0 to V4 and the set of the reference gray-scale voltages V5 to V9 fed from the MPX 61, and at the same time, causes a D/A converted signal voltage to be generated which is output through the voltage followers F1, F2, ..., F639, and F640 to each of the corresponding signal lines 22"; **page 6, paragraph 83, line 15 – page 7, paragraph 83, line (starting on page 7) 6];**

and a buffer receiving the calibrated image signal from the digital-to-analog converter

[Fig. 3 "voltage followers" **F1, F2, ..., F640** correspond to the "buffer receiving the calibrated image signals from the digital-to-analog converter"**].**

However, NOSE does not teach ***a data driver for a display forming an image frame composed of sub-frames of three primary colors by sequentially scanning horizontal lines for each sub-frame.***

HERRMANN teaches a "color sequential mode in which primary color images are displayed in successive frames". This mode is illustrated in **Fig. 2B** as "color sequential drive". HERRMANN teaches, "In the color sequential mode, the primary color signals are scanned into subframes of the display"; **page 2, paragraph 19, lines 1 – 2.** As shown in **Fig. 2B,** "each subframe of display 18 is updated at 3 or 4 times the field rate of 60 or 50 Hz and divided into alternate primary color subframes. The subframes comprise red, green, or blue video image signals"; **page 2, paragraph 19, lines 5 – 9.**

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine HERRMANN's teachings with those of NOSE as HERRMANN teaches that higher resolution can be obtained with reduced pixilation, "as each pixel can display full color using three scans" **[page 1, paragraph 4, lines 9 - 12**].

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Peter L. Cheng whose telephone number is 571-270-3007. The examiner can normally be reached on MONDAY - FRIDAY, 8:30 AM - 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, King Y. Poon can be reached on 571-272-7440. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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plc

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